ABSTRACT

Large, complex SoCs comprise interconnections of various functional blocks. Such functional blocks contain scan chains that are used for their individual production testing. The present invention utilizes these scan chains as a tool in the debugging of these SoCs by providing the internal contents of registers and memories contained on the SoC device. Accordingly, both hardware and software designers are provided a means to observe the effect of their designs on the internal operation of the SoC device. The invention is compatible with current integrated circuit design methodology and requires minimal area on the SoC for support circuitry.